**Lab 7: Flip-Flops**

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ECEN 328

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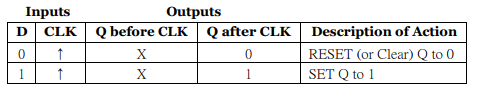
**Introduction:**

This lab was about teaching students about flip-flops. The student learned to examine the characteristics of the JK FF and the DFF, Examine the difference between synchronous and asynchronous inputs, examine the difference between level-triggering and edge-triggering, study the characteristics of J-K and D flip-flops with asynchronous inputs, create schematic designs for J-K and D FFs, including asynchronous inputs and test the designs on the target board. It teaches the students the significant of a clock and how to use it on the board in order to get results.

**Materials:**

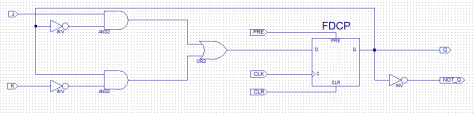
* Xilinx ISE software, student or professional edition V14.7
* Digilent Basys2 board with an XC3S100E device.

**Methods:**

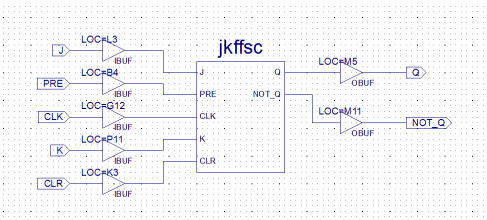
The student was asked to make a new project. The project was to be named d\_ff. The student is then to place a FD flip flop on the board and connect a D, Clk as input switches (SW0 and btn1) and an output of Q to LED1. The student was asked to test these results. They would find that the results are the same as: .

The section of this lab the student was asked to construct a jk flipflop. The student made a new project called jkff. The student made a new schematic called jkff. In the work space the student made a combinational circuit that would eventually turn into a flip flop for use. The student makes the internal circuit that is going to be converted into a jk flip flop. The student was to test the schematic with the created. The student was then asked to add the inputs of j, pre, clk, k, and clr with the outputs of Q, and not Q. The student is to record the results on the table.

**Data:**



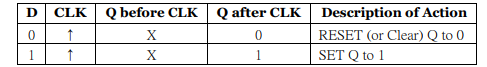
jkff internal



Jkff finished

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Pre | CLR | J | K | CLK | Q after ClK | Operation |
| 0 | 0 | 0 | 0 | ↓ | Hold | Synchronous |
| 0 | 0 | 0 | 1 | ↓ | 0 | Synchronous |
| 0 | 0 | 1 | 0 | ↓ | 1 | Synchronous |
| 0 | 0 | 1 | 1 | ↓ | Toggle | Synchronous |
| 1 | 0 | x | x | x | 1 | Asynchronous |
| 0 | 0 | x | x | x | 0 | Asynchronous |
| 0 | 0 | x | x | x | Not used | Invalid |

Table for the second section



**Truth table for part 1**

**Results and discussion:** The schematic is true to the truth table. We can see that from D flip works as a text book D flip flop should work. We almost see that with the JK flip flop. The student can see that we have a pre and clr work is fully functional. There are multiple functions that it can undergo as well.   
**Design challenge:**

* Are the asynchronous inputs PRE and CLR active-high or active-low?
  + Active low since it starts with 0 making it active
* Is this J-K FF positive edge or negative edge triggered?
  + The JK FF is negative edge triggered
* Which type of inputs, synchronous or asynchronous, has higher priority?
  + Synchronous
* What does “toggle” mean? Is its asynchronous operation?
  + Toggle makes to switch back and forth between Q and not Q
  + It is a synchronous operation

**Conclusion:**

The experiment above was based around flip flops and the overall applications.